SYSTEM AND METHOD FOR HANDLING LOAD AND/OR STORE OPERATIONS IN A SUPERSCALAR MICROPROCESSOR

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CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] The present application is related to the following applications, assigned to the Assignee of the present application: U.S. Patent Application SN 07/727,058, filed on July 8, 1991, (now abandoned) (attorney docket number SP021) by Nguyen et al. and entitled "EXTENSIBLE RISC MICROPROCESSOR ARCHITECTURE", and to a continuation of the '058 application SN 07/817,809, filed on Jan. 8, 1992, (now abandoned) which are herein incorporated by reference in their entirety.

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BACKGROUND OF THE INVENTION

Field of the Invention

[0002] The present invention relates generally to the design of a superscalar microprocessor and, more particularly, to a system and method for handling load and store operations in a microprocessor that executes instructions out-of-order.